CMOS sensor for face tracking and recognition

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ABSTRACT

This paper describes the main principles of a vision sensor dedicated to the detecting and tracking faces in video sequences. For this purpose, a current mode CMOS active sensor has been designed using an array of pixels that are amplified by using current mirrors of column amplifier. This circuit is simulated using Mentor Graphics^{TM}software with parameters of a 0.6 μm CMOS process. The circuit design is added with a sequential control unit which purpose is to realise capture of subwindows at any location and any size in the whole image.

Keywords: CMOS active sensor, embedded system, real time image processing

1. INTRODUCTION

A system capable of doing face localization and recognition in real time has many applications in intelligent man-machine interfaces and in other domains such as very low bandwidth video conferencing, and video e-mail.

This paper describes the main principles of a vision system, allowing to detect automatically the faces presence, to localize and to follow them in video sequences. Some preliminary works have shown that simplified RBF networks gave interesting results[1,2] but imposed a fast feature extraction to reduce the size of the input vectors of the RBF network. So, the main goal of the current project is the development and the characterisation of a specific CMOS sensor. A very large scale integration retina is proposed to realize the image acquisition, to extract a window of interest in the whole image and to evaluate means values of consecutive pixels on lines and columns.

A first image sensor with electronic shutter has been integrated in a 0.6 μm digital CMOS technology. The pixel cell consists of four transistors and a photodiode. Each pixel measures 30 μm by 30 μm and has a fill factor of about 40%. Each selected pixel produces a current which is transfered to the column readout amplifiers and multiplexed to the output of the sensor.

This retina also includes a logic command in order to realize acquisition of subwindows with random size and position. Actually, we are in a evaluation phase of this sensor.

Actual and future work will focus on the development of feature extracting architecture dedicated to the mean evaluation of consecutive pixel which will be used as input vectors of the RBF network.

2. ACTIVE PIXEL SENSOR

An active pixel sensor (APS) is defined as a detector array that has at least one active transistor within the pixel unit cell.[3] Currently, active pixel sensor technology integrates electronic signal processing and control with smart camera function onto the same single chip as a high performance image sensor.[4] CMOS image sensors with integrated signal processing have been implemented for a number of applications.[5] Most current CMOS imaging arrays have been designed for video applications, and digital photography. Improvement continues to be made in the growing digital image. A current mode image sensor has several advantages for example, low power supply, smaller place, higher operation speed.[6–8]

The following sections of this paper describe the design of the image sensor using a standard 0.6 μm CMOS process. The design is based on the integration of four MOS transistors for each pixel, a column readout amplifier, a sequential control unit which includes variable input counters, decoders, multiplexers and finaly an analog to digital converter. Also results based on simulation with Mentor Graphics^{TM}software are presented for each part of the circuit.

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3. SYSTEM ARCHITECTURE

The architecture of the proposed image sensor is shown in figure 1. This figure first describes the core of the system represented by the m x m array of transistors active pixels. On the left, the second block, the row decoder is charged to send to each line of pixels the control signals allowing pixel resetting, shutter opening or closing, pixel readout, ... On the botton of the circuit, the third block is made up of amplifiers, multiplexers and column decoders whose purpose is to detect, amplify and route the signal resulting from readout column to the output of the circuit. The automatic scan of the whole array of pixels or a subwindow of pixels is implemented by a sequential control unit which generates the internal signals to the row and column decoders. Finaly, the analogic output voltages are proportional to the gray scale intensity of the image. They are passed to analog to digital converter (ADC) (as seen on the right of the block diagram). This ADC allows the conversion of pixels analogic values in digital value which will be later processed by a DSP or a FPGA outside the acquisition system.

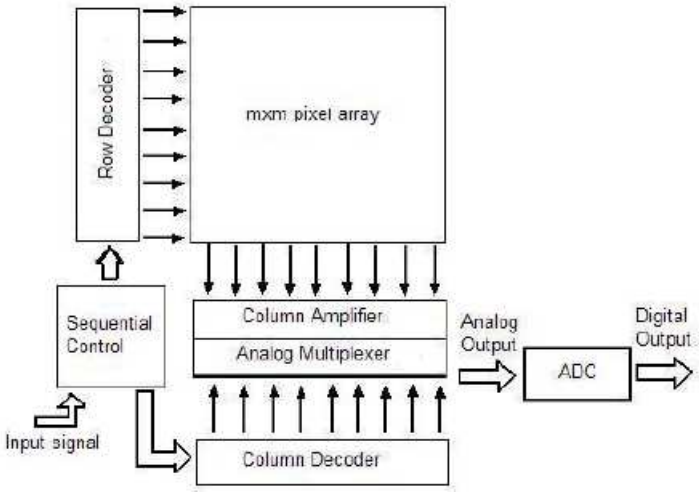

Figure 1. Image sensor system architecture

4. DESIGN AND SIMULATION

4.1. Active Pixel System

We used a standard pixel as described in the left part of figure 2 because it is a simple and stable design.[5, 9, 10] It consists of 3 PMOS transistors, a NMOS transistor for row access and a photodiode. *m_1* is the shutter transistor, *m_2* is the reset transistor, the transistor *m_3* acts as a transconductance buffer that converts the voltage at V_{pix} into a current. The vertical column lines in the array are implemented using second-layer metal. First layer metal is used for the horizontal row lines. Third-layer metal is connected to V_{ss} and covers all active areas of the pixel except the photodiodes.

Prior to the image acquisition, *m1* and *m_2* are on, resetting node V_{photo} and V_{pix} to the V_{reset} value. After reset, when *m_1* is on and *m_2* turned off, the charges generated by absorption of light are integrated onto the parasitic capacitances of the photodiode and the transistor *m_3*. So, during the exposure period, voltage is accumulated at node V_{photo} and V_{pix}. At the end of the exposure period, the shutter is closed by turning off *m_1*. Consequently, the photosignal is stored as a voltage on node V_{pix}. Finaly, during readout, the row access transistor *m_4* is turned on, and the drain current of *m_3* is fed via the column line to the column readout amplifier.

The right part of figure 2 shows the main waveforms (V_{Pix}, V_{Photo}, $V_{Shutter}$,V_{Reset},V_{Row} and V_{Col}) obtained during the simulation of one pixel. The pixels in a row are reseted by holding both reset and shutter low, turning on *m_1* and *m_2*. The voltages at nodes V_{photo} and V_{pix} are thereby reseted close to V_{reset}.
During exposure, reset goes high (*m_2* turns off) while shutter is unchanged at a low value (*m_1* remains on).

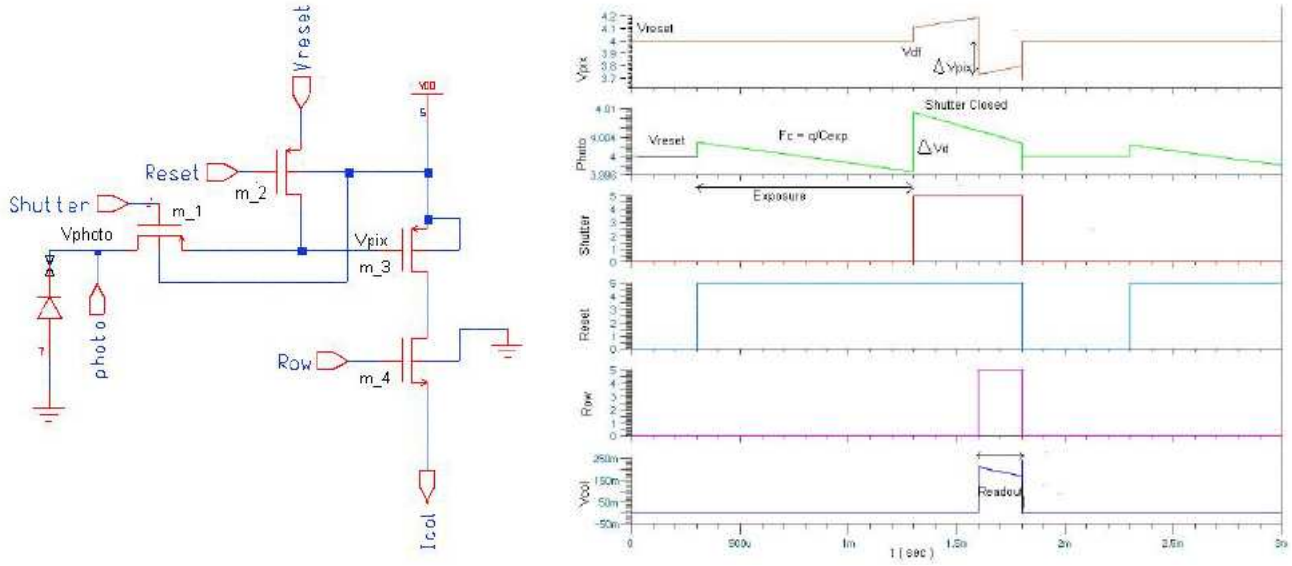

Figure 2. Pixel circuit schematic and results of simulation

So, the photocurrent can be integrated onto the parasitic capacitances at V_{photo} and V_{pix}. At the end of the exposure period, shutter is closed by turning off *m_1* and it is cutting off the photocurrent into the node V_{pix}. I_{col} can be read on the column bus when *m_4* is turned on (row is high). The voltage at the drain of *m_3* falls from V_{dd} to the bias voltage of the column line, and this change couples a small negative offset into node V_{pix}. The drain current of *m_3* is fed via the column line to the column readout amplifier.

The pixel circuit has been simulated with Mentor Graphics^{TM}software. The main result is shown on the figure 3, representing the values of the column current I_{col} as a function of the photodiode current I_{pix}. This figures highlights the quasi linearity of I_{col} for values of photodiode current from femto to picoamperes.

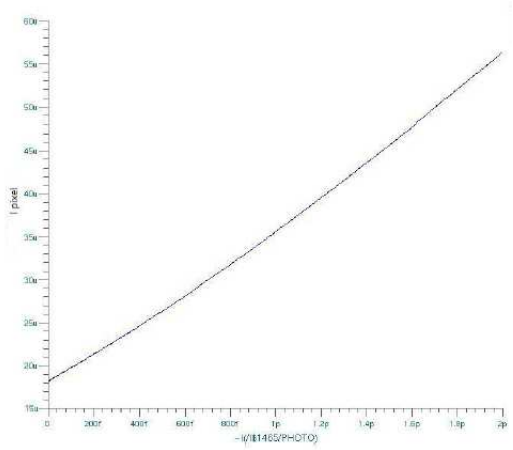

Figure 3. Simulated pixel current output

4.2. Column Amplifier

The figure 4 represents the electronic schematic of the column amplifier. The design of this amplifier provides a low impedance for the column lines, convert the readout current from the selected pixel into a voltage that is proportional to the integrated photovoltage in the pixel.

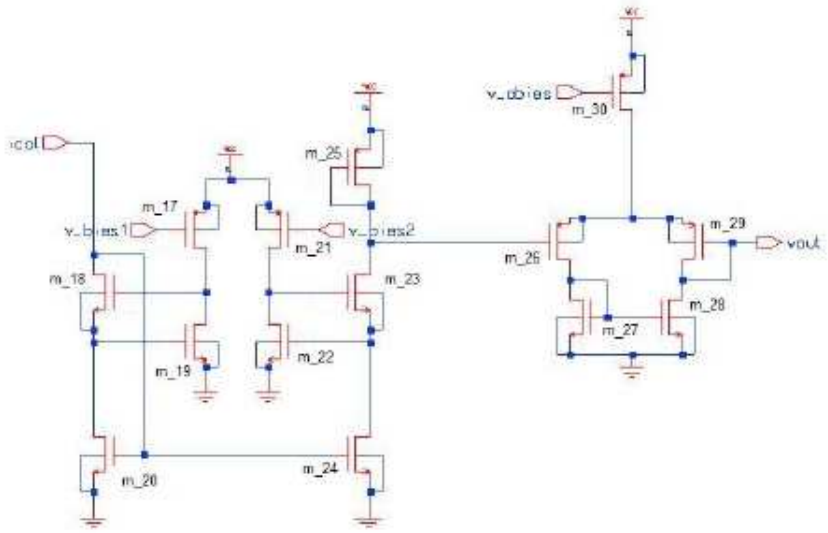

Figure 4. Column amplifier schematic

The concept of using current mirror amplifier column is to amplify signal by duplication at the column level. Amplification is achieved by designing current mirror m_{20} and m_{24} with ratio $W/L_{m_{20}} = n \times W/L_{m_{24}}$.

The transistors m_{22} and m_{23} are added to enhance the output impedance of the current mirror. The circuit including m_{17}, m_{18}, m_{20} operates almost identically to a diode-connected transistor, it is used to ensure that all transistor bias voltage are matched to the output side (m_{22}, m_{23}, m_{24}). The transistors m_{17}, m_{21} are used to bias the feedback circuit. The transistors m_{26}, m_{27}, m_{28}, m_{29}, m_{30} make up a differential unity gain amplifier. Once the current signal has been amplified by column current miroir amplifier, its output is suitable for any subsequent current mode image processing, either in continuous time or integration mode. In our case, these outputs will be used as inputs for the feature extracting architecture dedicated to the mean evaluation of consecutive pixels.

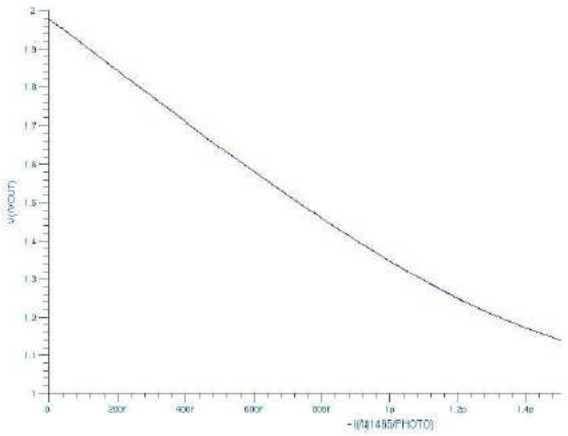

Figure 5. Simulated voltage output of the column amplifier

The pixel with its column amplifier has been simulated for a large range of photodiode currents as seen on figure 5. The output voltages are plotted as a function of input photocurrents. Good output linearity is observed, even at very low photocurrent.

4.3. Sequential Control

A framework dedicated to the sequential readout of successive rows and columns has been designed. The system offers the availability to program the location and the size of any window of interest in the whole image. Advantages of a such technology are large : random access of any pixel or subwindow, increase of acquisition frequency, ... In our main goal of face tracking, these aspects are crucial because only windows of interest will be scanned by the sensor, as illustrated in figure 6. This figure shows an acquisition of a subwindow of 4×4 pixels starting at the row 3 and column 4.

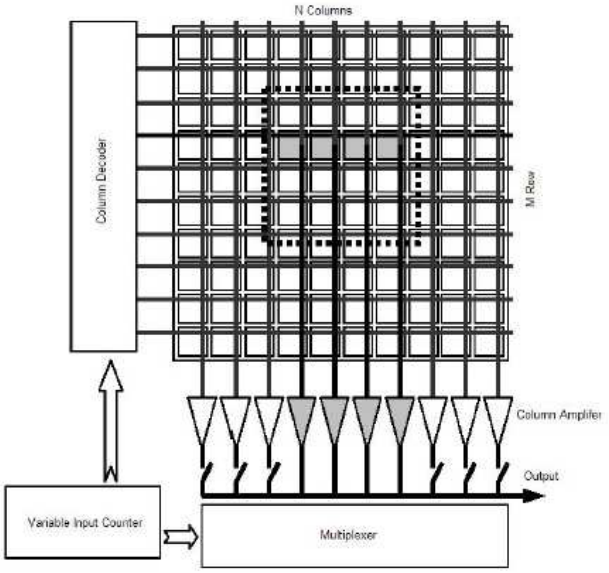

Figure 6. Readout of a window of interest

Each line of pixels follows the same sequence of reading but at different moments in order to multiplex the outputs. As seen in section 4.1, each pixel is controlled by 3 signals : reset signal, shutter signal and select signal. The figure 7 shows the readout sequence of 2 successive rows.

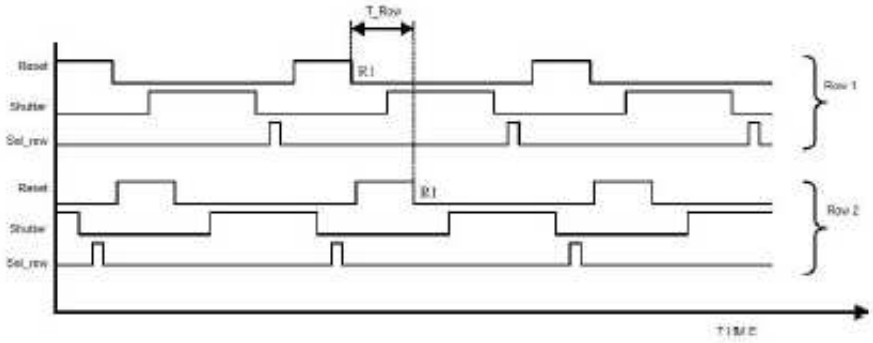

Figure 7. Timing diagram of the rows control signals

4.3.1. Variable Input Counter

To implement the sequential control, we need counters with variable inputs : the first for the starting position of the subwindow and the second for its ending position. Our design is inspired by a 74HC163 counter from Philips Semiconductors.[11] This circuit starts counting from a value which can be freely selected. It has been modified

in order to add the second input corresponding to the stop value of the counting process. An example of our 4 bits counter can be seen on the figure 8.

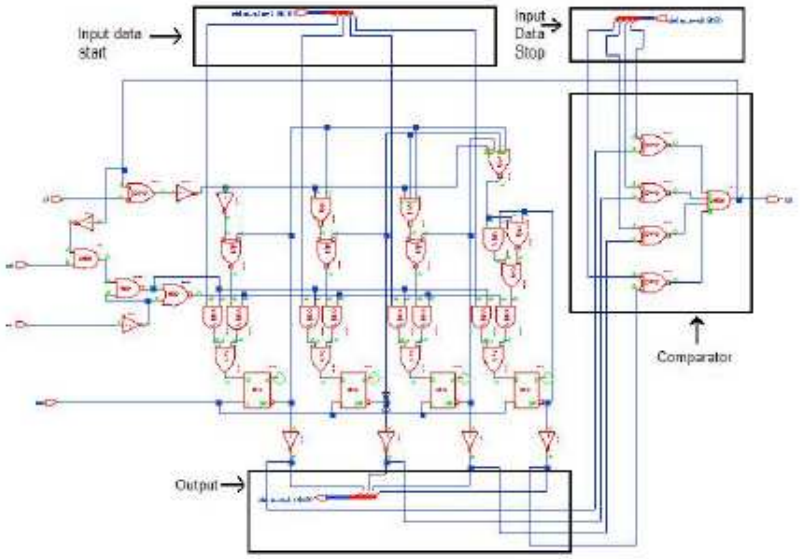

Figure 8. 4 bit Counter circuit

The figure 9 describes the results of the simulation of a such counter. There, it counts form a beginning value of 5 to an ending value of 14.

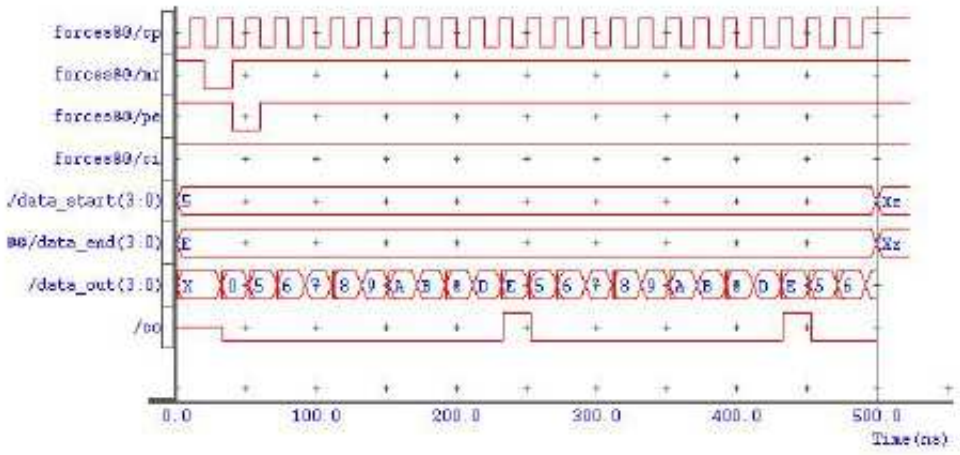

Figure 9. Simulated 4 bit counter

4.3.2. Decoder

The row decoder is used to active a pixels row. In this paper, row decoder is adopted from[12] . Row decoder sometimes called a tree decoder is shown in the left part of the figure 10. Two bits address a_0, b_0 are used to select one of the four outputs. The selected output is pulled high.

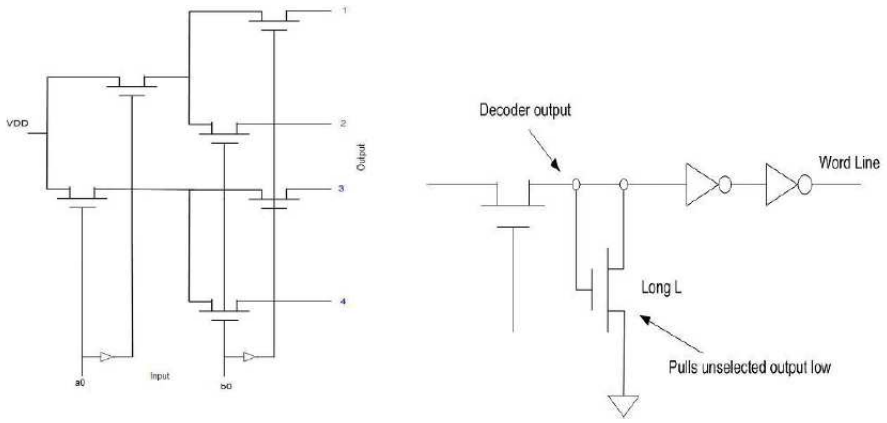

Figure 10. Row decoder

The right part of the figure 10 shows how the output of the decoder is pulled low when it is not selected. A long L mosfet is used to pull the output of the decoder low when that particular output is not selected. The result is that all decoder outputs are zero except for the output that is selected by the input address. Two inverters are used to drive the word line capacitance.

The two precedent circuits have been merged and lead to the transistors schematic of the complete decoder, as shown in figure 11.

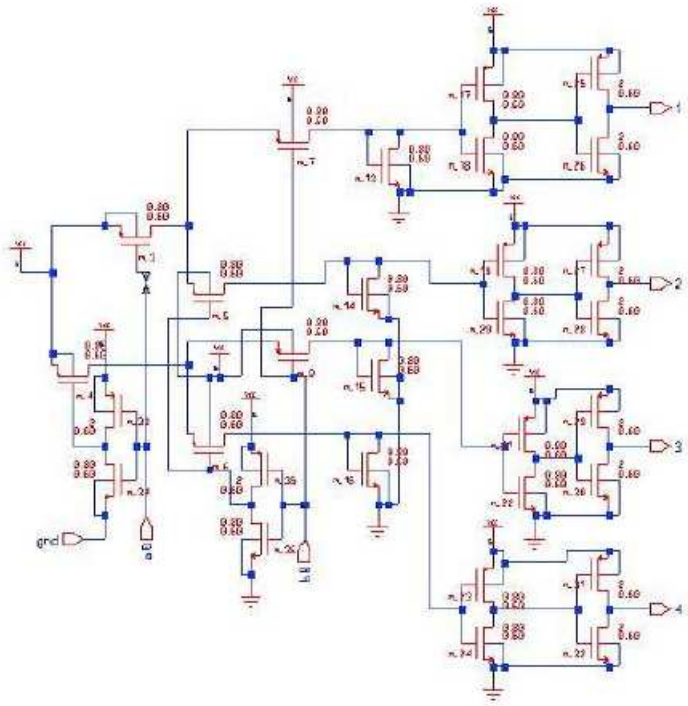

Figure 11. Complete decoder circuit

4.4. Multiplexer

Multiplexer is used to select and pass output voltage from column amplifier. It is controlled by output pixels counter. The figure 12 represents a simple design of this multiplexer. The analog switches only use a pair of transistors N/P.

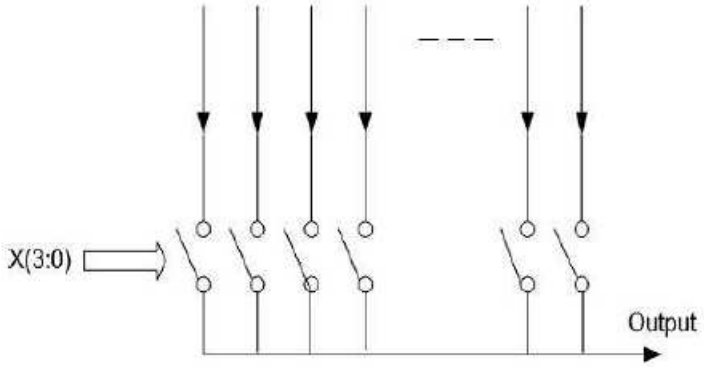

Figure 12. Multiplexer diagram

4.5. Analog To Digital Converter

The figure 13 shows a block diagram of a general pipelined ADC with n stages. Each stage contains a sample and hold (S/H), a comparator, a subtractor and an amplifier with a gain of two. The pipelined ADC is an N-step converter, with 1 bit being converted per stage. The pipelined ADC is able to achieve high resolution (10-13 bits) at relatively fast speeds.[12–14] The pipelined ADC consists of N stages connected in series. The algorithm of conversion at each stage can be seen on the figure 13.

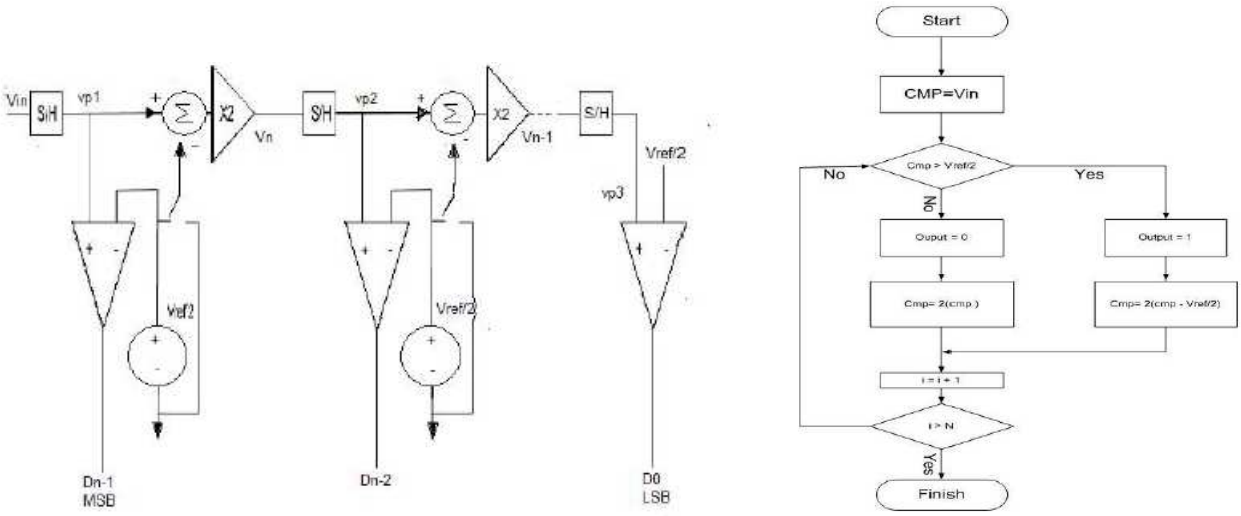

Figure 13. Pipelined ADC

After the input signal has been sampled, it is compared to $\frac{V_{ref}}{2}$. The output of each comparator is the bit conversion for that stage. If $V_{in} > \frac{V_{ref}}{2}$, the comparator output is 1, then $\frac{V_{ref}}{2}$ is subtracted from the held signal and the result is passed to the amplifier. If $V_{in} < \frac{V_{ref}}{2}$, the comparator output is 0, then the original input signal

is passed to the amplifier. The output of each stage in the converter is referred to as the residue. At the end, this residue is multiplied by 2 and the result is passed to the sample-and-hold of the next stage.

This ADC is currently in development and simulations are expected in a near future.

5. CONCLUSION

The design of a current mode CMOS active pixel image sensor with mode integration is presented in this paper. The circuit can work very well at small photocurrent. Current amplification is achieved through the use of current mirror in the amplification amplifier. The circuit has been designed and simulated on a standard 0.6 μm CMOS process.

Actual work focuses on the validation of the ADC design and the development of the feature extracting architecture dedicated to the mean evaluation of consecutive pixels.

The next effort will be the fabrication of the real chip on a standard 0.6 μm or 0.35 μm CMOS process. Evaluation and comparaison of fabricated chip will be conducted refer to theoretical and simulated results.

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